ANALYSIS AND DESIGN OF GaAs MESFET MIXERS

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Abstract

A generalized approach to the analysis of GaAs MESFET mixers has been developed, which accurately calculates the input and output impedances and stability conditions, and is applicable to upconverters and harmonic mixers. Two mixer designs are presented along with experimental results yielding conversion gains of 6 and 11 dB, noise figures of 4.5 and 5.5 dB, and third-order intermodulation intercepts of 12 and 15 dBm, respectively. These are state-of-the-art results for single gate FET mixers.

Introduction

In the past few years several approaches to the analysis of GaAs FET mixers have been presented [1]-[5]. All of these analyses use simplifying assumptions which limit their application to simple downconverters or low IF frequencies. Since these analyses make use of highly simplified FET equivalent circuits, they can not be used to determine input or output impedances or stability. The analysis which has been developed is useful for harmonic mixers, upconverters, or mixers with unusual frequency combinations or other operating parameters, as well as simple downconverters. These results have been obtained through the use of an improved FET equivalent circuit, which leads to greater accuracy and allows determination of input impedance and stability.

The GaAs FET model and mixer analysis

The analysis is based on a lumped quasi-static FET equivalent circuit; the values of the circuit elements are determined by a least-squares fit of measured S parameters at multiple bias voltages, where appropriate, and by an analytical FET model. The gate/drain and gate/source capacitances and the drain current are treated as nonlinear functions of drain and gate voltage, and the source and load impedances can be specified arbitrarily at any frequency. The time waveforms for the nonlinear elements are first found under LO excitation only, using an iterative procedure similar to [6]. Conversion matrices [7] are then used to describe the time-varying elements in the frequency domain, and conversion gain and input/output impedances are calculated.

Experimental results

Two mixers were designed and characterized. The first uses an Avantek AT8251 FET chip and was designed primarily to verify the analysis. The second uses a packaged Avantek AT8060 FET and is a practical component with 500 MHz instantaneous bandwidth. Both have an RF center frequency of 8.2 GHz with a 1.2 GHz IF and fixed 7.0 GHz LO, and similar matching circuits. The input matching circuit is designed to match the FET at the RF frequency using a simple stub matching section. The input circuit also short-circuits the FET gate at the IF frequency, to guarantee stability and to prevent excessive gain and noise at the IF. The image frequency is similarly mismatched. The LO signal is applied to the same port as the RF via a filter diplexer. The output network uses a four-section low-pass filter to reject the LO and to present a short to the drain at all frequencies except the IF; the optimum IF termination at the drain was found to be approximately 70 ohms, real, for both mixers. Since the output impedance of a FET mixer is invariably quite high, due to the high average impedance of the drain/source resistance, it is possible to increase conversion gain by increasing the load impedance. Stability may suffer, however, if the gain is made too high.

The first mixer was designed using a computer program embodying this analysis. The results indicated that the input and output impedances of the FET at all mixing frequencies had positive real parts for all passive source and load impedances, and predicted the conversion gains eventually obtained. The measured conversion gain and that calculated from measured source and load impedances of the first mixer are presented in Figure 1. The accuracy observed at high LO power levels results from the inclusion and accurate characterization of the FET's capacitive nonlinearites and drain/source resistance. The measured and calculated input impedances at the FET gate are 4-j36 and 4-j39 respectively. The single-sideband noise figure of this mixer was below 5.9 dB for LO power between

-3 dBm and 6 dBm, with a minimum of 5.5 dB from -2 to 3 dBm. The output third-order intermodulation intercept point is 15 dBm at 9 dBm LO power.

The second mixer was designed using the same methodology as the first, but its performance was not calculated from measured source and load impedances. Its measured conversion gain and noise figure over its 500 MHz bandwidth are shown in Figures 2 and 3; minimum noise figure was achieved with a matched RF input. The output intermodulation intercept for this mixer was 12 dBm at 6 dBm LO power, and dropped approximately 1.5 dBm for each dB reduction in LO level. The input VSWR was below 2.1 over the passband.

All data for each mixer was recorded with the same bias and tuning conditions, and stable performance was observed at all LO power levels within the operating range, and at all passive load impedances. This performance is superior to any reported for single-gate FET downconverters in this frequency range, and is far superior to that obtainable from diode mixers.

References

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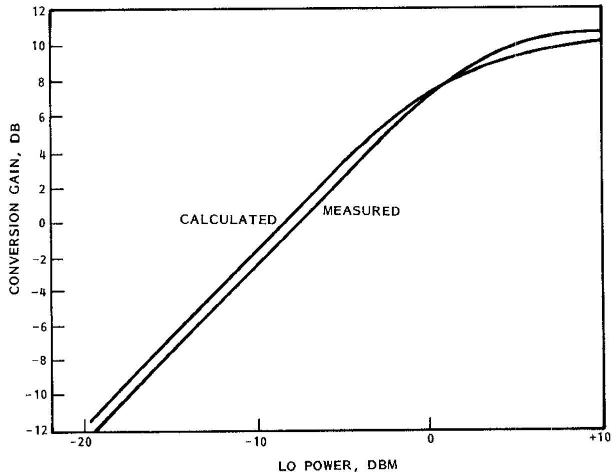

Figure 1. Measured and calculated conversion gain.

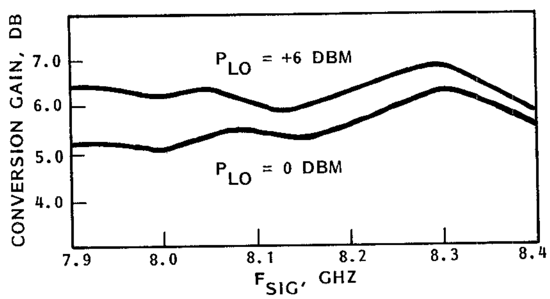

Figure 2. Conversion gain of mixer no. 2.

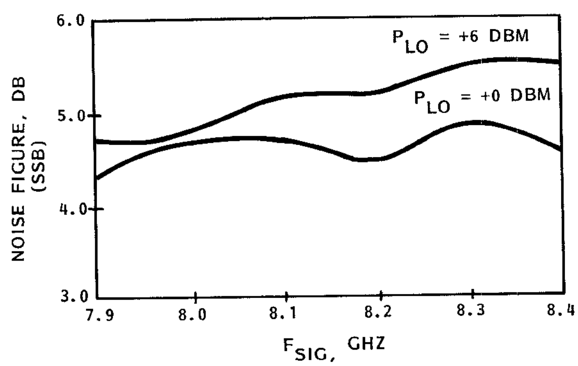

Figure 3. Noise figure of mixer no. 2.